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(54) **Phase-locked loop system with compensation for data-transition-dependent variations in loop gain.**

(57) The loop gain of a phase locked loop (10) is made to be controllably responsive to the transition density of an input data signal. In one embodiment a charge pump (16), positioned between the phase detector (14) and the loop filter (18), supplies pulse-amplitude-modulated current pulses to the loop filter, the amplitude of pulses being related to the data transition density.

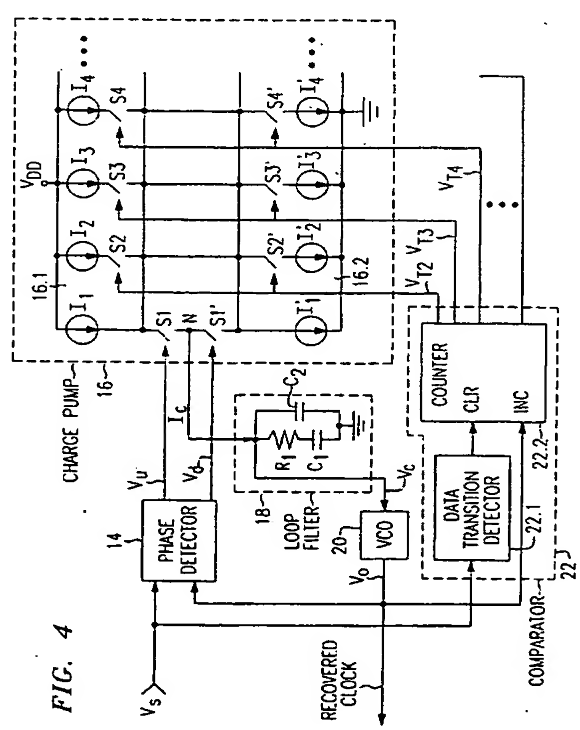

FIG. 4

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Background of the Invention

This invention relates to phase locked loop (PLL) systems in which the density of data transitions in the data signal varies.

Monolithic PLL circuits have become the basic building blocks of many consumer and industrial electronic systems. In telecommunication data systems, for example, the PLL is an integral part of the clock recovery subsystem. The PLL may be used to recover the clock signal from the data signal; the recovered clock may then be used, for example, to regenerate the data signal.

The basic PLL system generally comprises three elements: (1) a phase detector, (2) a loop filter, and (3) a voltage controlled oscillator (VCO), which are interconnected in a feedback system as shown in FIG. 12.1 of "Bipolar and MOS Analog Integrated Circuit Design," A. B. Grebene, John Wiley & Sons (1984). The phase detector compares the phase of an input signal V_s with the phase of the VCO and generates a control voltage V_d. This voltage V_d is filtered by the loop filter, the output of which is applied to the control terminal of the VCO to control its frequency of oscillation.

The loop gain, K_L, of the PLL is defined as follows:

$$K_L = K_D K_o \quad (1)$$

where K_D (V/rad) is the phase detector conversion gain, and K_O (HZ/V) is the voltage-to-frequency conversion gain of the VCO.

It is well known that the phase detector gain K_D, and hence the loop gain, of a clock recovery PLL is dependent on the transition density of the data signal. (D.L. Duttweiler, BSTJ, Vol. 55, No. 1 (1976)). That is, when the data signal undergoes few data transitions, the phase detector has periods of time when no data transitions occur to compare with the VCO recovered clock. The effective phase detector gain K_{DD} is then degraded by a factor D < 1 defined as

$$D = f_{trans} / f_{clk} \quad (2)$$

and

$$K_{DD} = K_D D \quad (3)$$

where f_{trans} is the frequency of the data transitions and f_{clk} is the frequency of the recovered clock.

Consider two cases illustrated by FIGS. 1 and 2. In both cases the PLL is locked to an input data signal, but the clock signal is lagging the data signal by a phase error Δ. In FIG. 1, there is only one rising clock cycle transition between adjacent data transitions; thus, the degrading factor D = 1. But, in FIG. 2, there are three rising clock cycle transitions between adjacent data transitions; thus D = 1/3. Therefore, there are three times the number of error corrections in the D = 1 case than in the D = 1/3 case. This difference effectively makes the phase detector gain of FIG. 2, K_{D2} = 1/3 K_{D1}, where K_{D1} is the phase detector gain of FIG. 1, even though the phase detectors themselves have physically the same implementation.

This data-dependent variation of the phase detector gain will cause variations in the PLL closed loop dynamics and may be undesirable. For example, in a second order active loop filter PLL (Grebene, supra, FIG. 12.9), the natural frequency, the damping factor and the 3dB frequency all decrease as K_{DD} decreases, but the jitter peaking increases. This effect is particularly troublesome in systems in which the PLLs (or repeaters which include the PLLs) are cascaded. For example, in token ring systems data may be inserted/extracted at different nodes such that different repeaters/PLLs see different data streams. With prior art PLLs, the transfer function of the PLL shifts with transition density such that some PLLs may lose lock; others may not.

Summary of the Invention

The invention is as set out in the claims.

The loop gain of a PLL is made to be essentially constant by compensating for the dependence of that gain on the data transition density of an input data signal. The loop gain is made to be controllably responsive to the transition density of the input data signal so as to increase the loop gain when the density is relatively low and, conversely, to decrease the gain when the density is relatively high. In one embodiment of this method, the number of clock transitions (either rising or falling) between adjacent data transitions is counted and used to adjust the loop gain. In a preferred embodiment, the average loop gain is essentially constant with changes in transition density.

This method is illustratively implemented in a PLL which includes a modulator for altering the loop gain in response to the difference between the data transition density of the input signal and the clock signal. Illustratively the modulator comprises a charge pump located between the phase detector and the loop filter. The charge pump supplies current pulses to the filter, the amplitude of the pulses being related to the data transition density; the lower the data transition density in a given time interval, the higher the pulse amplitude (and conversely).

The invention is particularly attractive for use in systems in which there is an upper bound on the number of data bits which can occur without a data transition also occurring. Examples of such systems are those employing Manchester coding or Run Length Limited coding schemes.

It is also attractive for use in systems where the PLLs are cascaded because the PLL transfer functions, like the loop gain, are independent of transition density and, so, regardless of what data stream a PLL sees, it always maintains the locked condition.

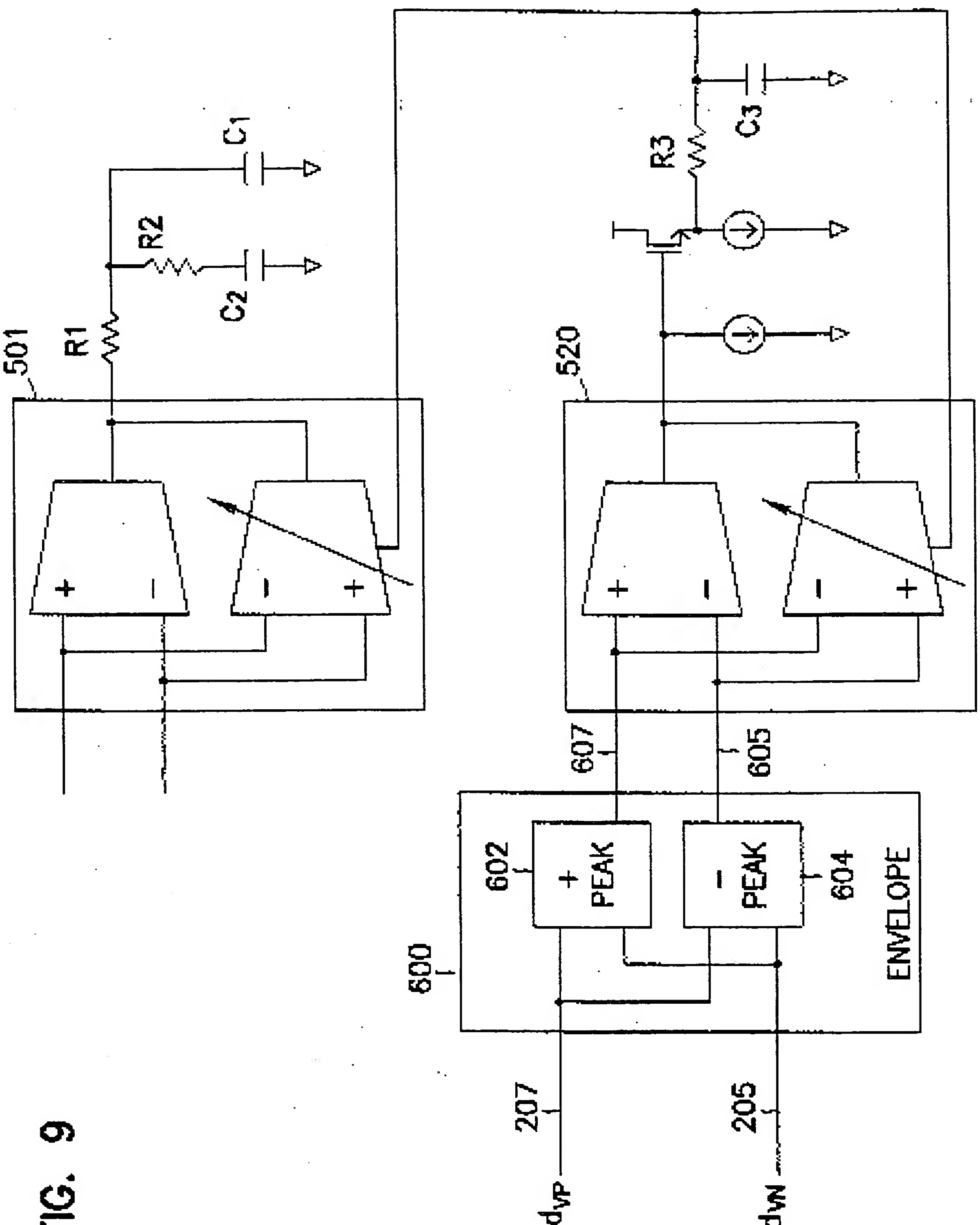

501
R1
R2
C2
C1
520
R3
C3
607
605
602
+ PEAK
− PEAK
604
600
ENVELOPE
207
205
d_{VP}
d_{VN}

FIG. 9

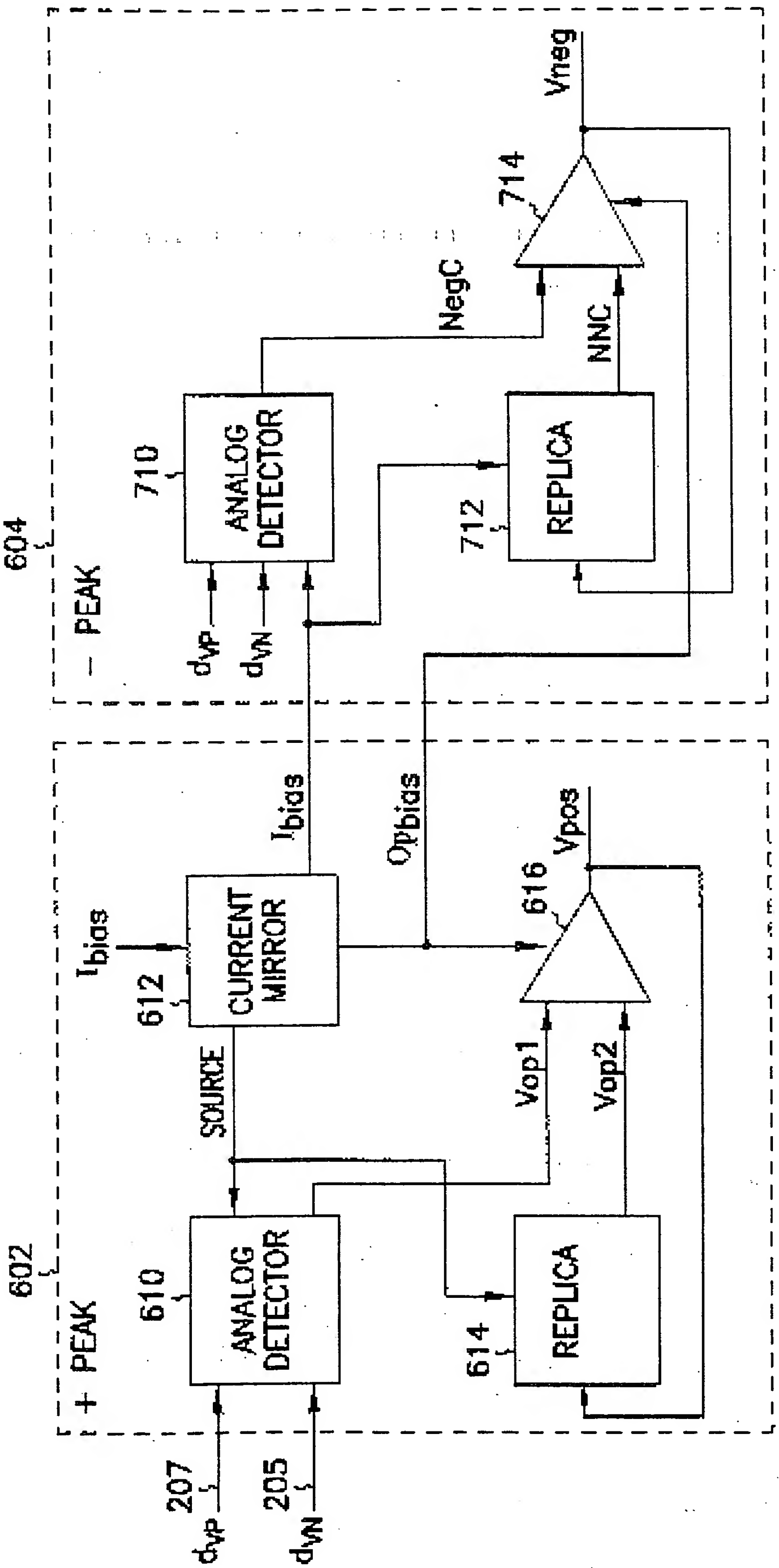
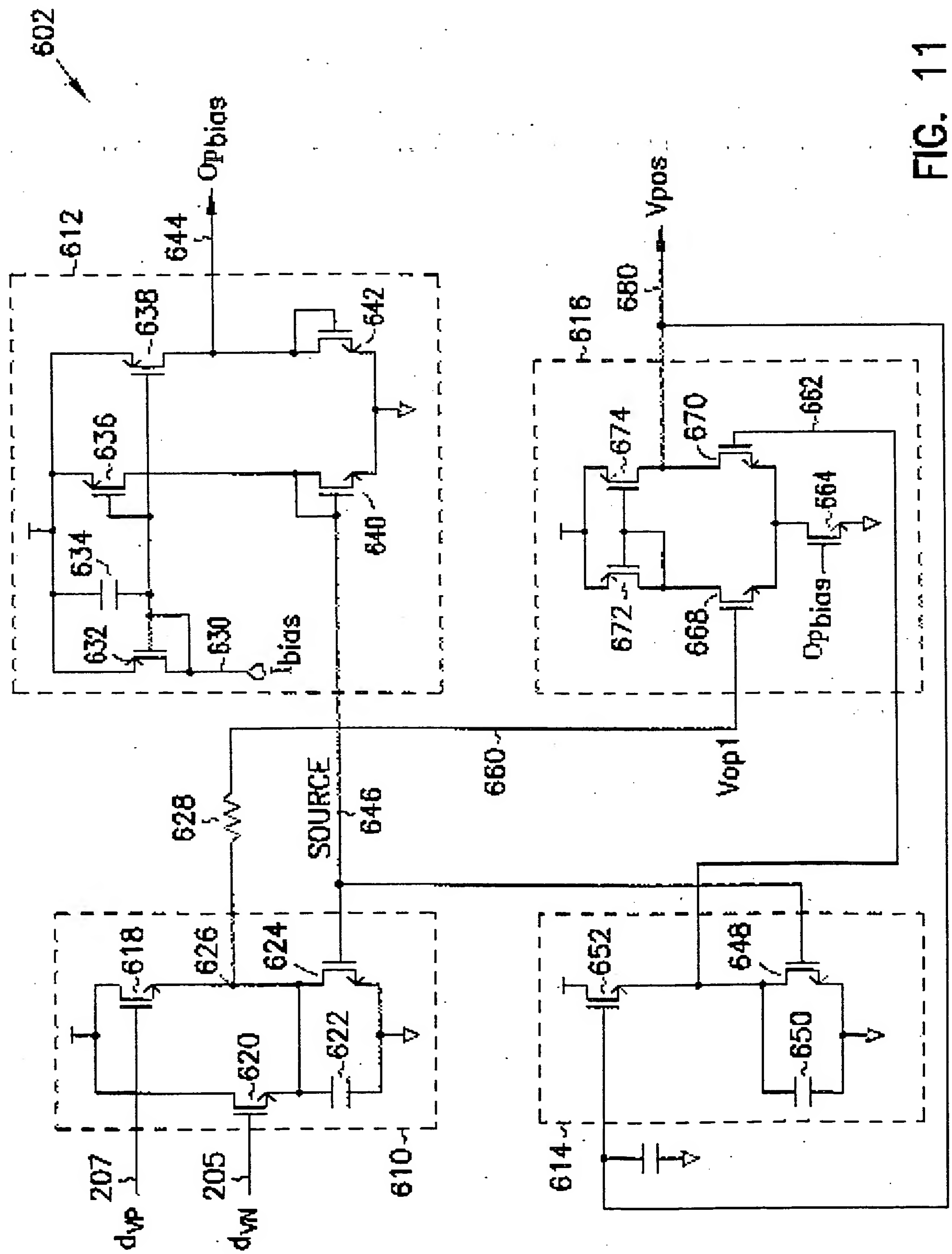

604
– PEAK
710
ANALOG DETECTOR
d_{VP}
d_{VN}
NegC
714
Vneg
712
REPLICA
NNC
602
+ PEAK
610
ANALOG DETECTOR
207
205
d_{VP}
d_{VN}
612
CURRENT MIRROR
I_{bias}
SOURCE
I_{bias}
Op_{bias}
616
Vpos
Vop1
Vop2
614
REPLICA

FIG. 10


602
612
644
Opbias
638
636
642
634
632
630
Ibias
640
616
680
Vpos
674
670
662
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672
668
Opbias
660
Vop1
628
SOURCE
646
618
626
624
620
622
207
d_{VP}
205
d_{VN}
610
652
648
650
614

FIG. 11

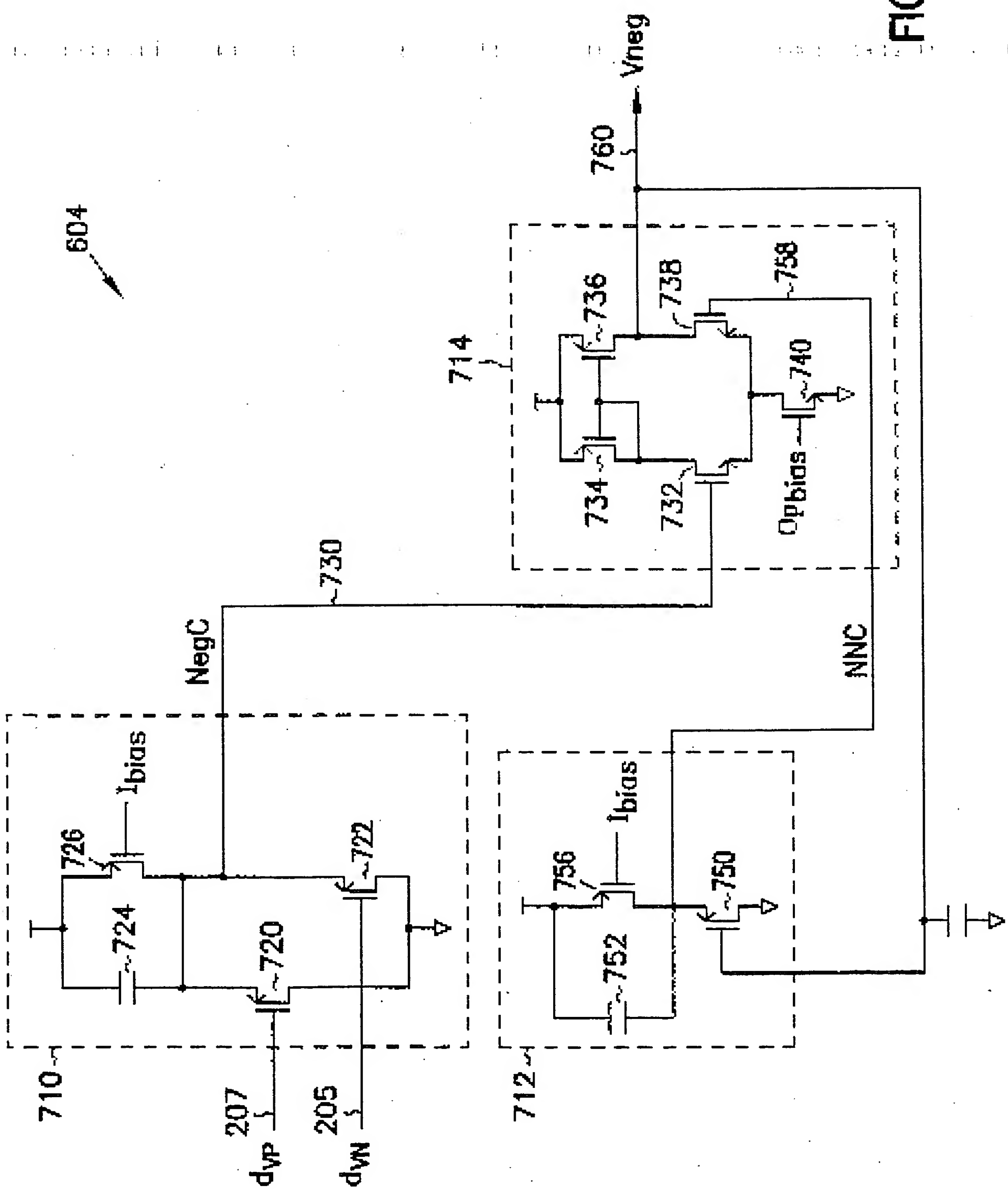

604
714
736
738
758
760
Vneg
740
734
732
Opbias
730
NegC
NNC
Ibias
726
724
720
722
710
207
dVP
205
dVN
Ibias
756
752
750
712

FIG. 12

coupled through switch S1 to node N for delivering a positive current control pulse I_c of amplitude nI (n=1, 2, 3...) to the loop filter, and, similarly, a second bank 16.2 of parallel-connected current sources I'_i (i = 1, 2, 3...) coupled through switch S1' to node N for delivering a negative current control pulse I_c to the loop filter. The amplitude of the current pulses is determined by the number of switches S_i or S'_i (i = 2, 3, 4...) which are closed under control of V_{Ti}, whereas the duration (width) of the current pulse I_c is determined the length of time that switches S1 or S1' are closed under control of the phase detector outputs V_u and V_d, respectively. Thus, the width of the current pulses I_c is related to the phase error generated by the phase detector and as a result may vary considerably (e.g., 0-50%). In the interest of simplicity, however, FIG. 5 shows the pulses I_c to be of equal duration.

In operation of the embodiment of FIG. 4, the phase detector 14 compares the rising edge (for example) of the clock signal V_o to a data transition of input signal V_s. Assuming a positive VCO gain K_o and an "early" clock transition, then a pulse would be generated on the "down" output V_d. This pulse would cause the control voltage V_c to decrease, thus slowing the frequency of V_o (i.e., the clock rate). Note, however, the clock in FIG. 5 is shown to have a constant frequency in the interests of simplicity (i.e., in many cases the actual frequency shift would be imperceptible in a schematic drawing). Conversely, if the clock transition were "late", a pulse would be generated on the "up" output V_u to accelerate the clock rate.

Consider now the operation of charge pump 16 in which we assume each current source supplies a current of magnitude I. A pulse on V_u closes switch S1 and connects bank 16.1 to loop filter 18. The amplitude of the control current I_c supplied to the filter is I + kI; that is I (from I_1) plus kI (k = 0, 1, 2...) depending on how many of the switches S_i (i = 2, 3...) are closed. The duration of I_c is dependent on the duration of V_u. Similar comments apply to a pulse V_d applied to switch S1'. In both cases counter 22.2 controls the closure of switches S_i and S'_i (i = 2, 3...) by counting the number of clock transitions which occur between adjacent data transitions. If a data transition occurs (t_o, FIG. 5), transition detector 22.1 clears the counter 22.2 and V_{Ti} (i = 2, 3...) are all set to zero, thus disabling the current sources I_i and I'_i (i= 2, 3...). If a data transition occurs after t_o, the current source I_i or I'_i supplies the necessary control current. However, if no data transition occurs by the second rising clock edge at t_1, as shown in FIG. 5, then V_{T2} goes high on the trailing edge of that clock cycle (at t_2) which closes switches S_2 and S'_2 and prepares I_2 and I'_2 for injection of control current into the loop filter. (As noted earlier, whether the positive control current I_2 or the negative one I'_2 is injected depends on whether a pulse appears on V_u or V_d.) Similarly, if there continues to be no data transition by t_3, the rising edge of the third clock cycle, then at t_4 V_{T3} goes high, closes S_3 and S'_3 so that current sources I_3 and I'_3 are prepared to inject current into the loop filter. Note, during the interval t_o - t_5 when there is no data transition, both V_u and V_d are low, the third state of the tri-state phase detector. Finally, when a data transition occurs at t_5, the phase detector detects the transition and applies a control voltage V_d to the charge pump so that a control current pulse I_c = -3I is applied to the loop filter. In a similar fashion, FIG. 5 shows, for example, additional control current pulses of amplitude +2I, -I, +4I, -I, -I, and +I, respectively, being generated by the charge pump at times t_6 to t_{11}, respectively. In this manner, the phase detector gain, and hence the loop gain, is adjusted to compensate for the changing transition density of the data signal.

It is to be understood that the above-described arrangements are merely illustrative of the many possible specific embodiments which can be devised. For example, there are many alternative designs of counter 22.2 well-known in the art which would be suitable for use in the inventive PLL system. One such design is shown in FIG. 6 wherein a plurality of D-flip flops are arranged in tandem. A dc voltage corresponding to a logic state is applied to the D input of the first flip flop, and the control voltages (V_{Ti}) (i = 2, 3...) are taken from the Q outputs of the respective flip flops. The increment signal INC from the VCO is applied to the clock inputs CLK of the flip flops, and the clear signal CLR from the data transition detector 22.1 is applied to their clear inputs.

In addition, although the foregoing description relates, for illustrative purposes, to analog PLL systems, the principles of the invention are also applicable to all-digital PLLs, e.g., a PLL with a digital loop filter and digital phase detector, a PLL implemented in an FPGA or a DSP, or a PLL implemented in software in a microprocessor.

Finally, it should be noted that the invention is advantageously used in systems where the data is coded so that there is an upper bound on the number of data bits which can occur between data transitions. Examples of such coding schemes are Manchester coding and Run Length Limited coding. However, the invention is not limited to such use in such systems. Thus, if the embodiments of the invention shown in FIG. 3 or FIG. 4 were used in system without an upper bound of the type described above, then the PLL would still provide loop gain compensation, and hence be an improvement over the prior art, up to the point where the charge pump had already switched in the maximum number of current sources provided by the physical design even though a relatively low transition density data signal may be "demanding" more current.

Brief Description of the Drawings

The invention, together with its various features and advantages, can be readily understood from the following more detailed description taken in conjunction with accompanying drawing, in which:

FIGS. 1 and 2 are waveforms used to describe the adverse effect of data transition dependent gain on PLL performance;

FIG. 3 is a block diagram of a PLL system in accordance with one embodiment of the invention;

FIG. 4 is a combined block diagram and circuit schematic of the embodiment of FIG. 3;

FIG. 5 shows waveforms useful in explaining the operation of the embodiment of FIG. 4; and

FIG. 6 is an illustrative implementation of the counter of FIG. 3.

Detailed Description

As noted above, the invention in general makes the loop gain of a PLL system controllably responsive to the transition density of a data signal. In particular, the invention makes the loop gain essentially constant even though the transition density may vary.

A block diagram of a PLL system 10 in accordance with one embodiment of the invention is shown in FIG. 3. The system includes a feedback loop 12 formed by a phase detector 14, a loop gain modulator (e.g., a charge pump 16), a loop filter 18, and a voltage controlled oscillator (VCO) 20. Located outside the loop 12, a data transition comparator 22 compares the transitions of the input data signal V_s with those of the clock V_o (i.e., the VCO output) and generates pulse width modulated (PWM) control pulses V_T. The PWM pulses V_T control the magnitude of pulse amplitude modulated (PAM) current pulses I_c supplied by charge pump 16 to loop filter 18. The latter, in turn, generates a control voltage V_c which controls the frequency of VCO 20. Loop filter 18, which may be active or passive, VCO 20, which may be a relaxation oscillator, and transition comparator 22, which may simply be a differentiator followed by rectifier, are all well-known in the art.

Phase detector 14 may be any one of a class of well known detectors suitable for handling non-periodic data signals. As shown in FIG. 3, phase detector 14 has two inputs: the input data signal V_s and the output signal (clock) V_o of VCO 20. Detector 14 compares the phases of V_s and V_o and generates two outputs, V_d and V_u, but three allowable states. That is, these outputs are logic levels applied to the charge pump 16: (1) V_u alone is true when the output frequency of VCO 20 needs to be increased, (2) V_d alone is true when the output frequency of VCO 20 needs to be decreased, and (3) V_u and V_d are false simultaneously when the output frequency of VCO 20 is to remain unchanged. Both V_d and V_u are never true simultaneously. This type of tri-state phase detector used in conjunction with a charge pump is described by F. M. Gardner in an article entitled "Charge-Pump Phase-Lock Loops," IEEE Transactions on Communications, Vol. COM-28, No. 11, p. 1849 (1980). Although Gardner describes the charge pump as "nothing but a three-position, electronic switch that is controlled by the three states" of the phase detector, in our PLL the combination of the charge pump 16 and the data transition comparator 22 function in a unique manner to supply PAM current pulses I_c to the loop filter 18. The amplitude of these pulses is related to the transition density of the input data signal V_s. Since the transition density changes as a function of time, the PLL dynamically adjusts the current pulse amplitudes so that the phase detector gain, and hence the loop gain, compensates for variations in density. Effectively, therefore, the gain and hence the loop dynamics are maintained essentially constant over a relatively wide range of data transition densities.

The effective phase detector gain (and hence the loop gain) is dynamically adjusted by means of charge pump 16 and comparator 22. The comparator 22 counts the number of clock cycles n which occur between data transitions and generates a suitable control signal V_T which enables the charge pump 16 to deliver a current pulse of amplitude nI to the loop filter 18. For example, in FIG. 2 (the case of a degrading factor of D = 1/3) during the interval t_o - t_1, three clock cycles have occurred before the data transition at t_1. Consequently, the comparator 22 supplies a suitable control signal V_T to charge pump 16 so that a current pulse of amplitude 3I (not shown in FIG. 2) is applied to the loop filter at approximately t_1. The sign of the pulse may be either positive or negative depending on whether the clock signal is lagging or leading the data signal, respectively.

The manner in which the PAM control current is generated can be better understood from the following more detailed description of FIGS. 4-6 in which corresponding components of FIG. 3 and FIG. 4 have been given identical reference numerals. In this embodiment the loop filter 18 is a standard second-order filter having the series combination of a resistor R_1 and a capacitor C_1 connected between its input terminal and ground, with smoothing capacitor C_2 connected in parallel with the R_1-C_1 combination. On the other hand, the data transition comparator 22 comprises a data transition detector 22.1 (e.g., a differentiator followed by a rectifier) with its input coupled to V_s and its output coupled to the clear input CLR of counter 22.2. The increment input INC of the counter is coupled to V_o, whereas the parallel outputs of the counter are control voltages V_{Ti} (i = 2, 3, 4...) coupled to the charge pump 16 so as to control the state of switches S_i and S'_i (i=2, 3, 4 ...).

The charge pump itself includes a first bank 16.1 of parallel - connected current sources I_i (i = 1, 2, 3...)

15. A phase-locked loop subsystem for locking an input data signal to a clock signal comprising

an oscillator (20) for generating said clock signal in response to a first control signal,

a phase detector (14) for comparing the phase of said input signal with that of said clock signal and for generating second control signals in response to the comparison,

CHARACTERISED BY:

a comparator (22) for counting the number of rising (or falling) clock signal transitions which occur between adjacent data signal transitions to generate third control signals, the durations of said third control signals being related to said numbers,

a low pass filter (18), the output of said filter providing said first control signal to said oscillator, and

a current source (16) for injecting amplitude modulated current pulses into said filter, the timing of said pulses being responsive to said second control signals from said phase detector, and the amplitude of said pulses being responsive to said third control signals from said comparator and being effective to maintain the loop gain essentially constant with changes in the transition density of said input signal.

Claims

1. A method of operation of a phase-locked loop system for locking an input data signal to a clock signal, CHARACTERISED BY:
   (a) counting the number of clock signal transitions which occur between data signal transitions, and
   (b) altering the loop gain of said system in response to said counting step (a).

2. The method of claim 1 wherein, in step (b) the average loop gain is maintained essentially constant with changes in transition density of the input signal.

3. The method of claim 1 wherein said system includes a phase detector for comparing the phase of said input signal to that of said clock signal and wherein step (b) includes altering the effective gain of said phase detector, in response to said counting step (a).

4. The method of claim 3 wherein said system includes a loop filter for filtering the output of said phase detector and wherein step (b) includes injecting current pulses into said loop filter, the amplitude of said pulses being related to the number of said transitions counted in step (a).

5. The method of claim 4 wherein said injecting step includes using the output of said phase detector to determine when said current pulses are injected into said loop filter.

6. A method of locking a data input signal to a clock signal comprising the steps of:
   (a) generating said clock signal,
   (b) comparing the phase of said data signal with that of said clock signal to generate a first control signal, said comparing step having a characteristic gain measured in volts per radian,
   (c) modulating the frequency of said clock signal in response to said first control signal, CHARACTERIZED BY:
   (d) counting the number of rising (or falling) clock signal transitions which occur between adjacent data signal transitions, and
   (e) altering said gain in response to said counting step.

7. The method of claim 6 wherein, in step (e) the gain is altered in a manner to maintain it essentially constant with changes in the transition density of said input signal.

8. The method of claim 6 wherein step (e) includes generating current pulses in response to said first control signal, the amplitudes of said pulses being related to the numbers counted in step (d), and the modulation of said clock signal frequency in step (c) being responsive to said current pulses.

9. A data system comprising
   a phase-locked loop subsystem (10) for locking an input data signal (V_s) to a clock signal (V_0), said loop subsystem having a characteristic loop gain related to the difference in phase between said input signal and said clock signal, CHARACTERISED BY:
   a modulator (16, 22) for altering said loop gain in response to the difference between the data transition density of said input signal and that of said clock signal.

10. The system of claim 9 wherein said modulator alters the loop gain in a manner to maintain said gain essentially constant with changes in the density of said input signal.

11. The system of claim 9 wherein said modulator includes
   a comparator (22) for generating a first control signal (V_T) related to said difference in data transition density, and
   a source (16) for injecting current pulses into said loop in response to said first control signal.

12. The system of claim 11 wherein
   said comparator counts the number of rising (or falling) clock signal transitions between adjacent data signal transitions, and
   said source injects pulses the amplitudes of which are related to said numbers counted by said comparator.

13. The system of claim 12 wherein
   said loop subsystem includes a tri-state phase detector (14) for generating second control signals responsive to the difference in phase between said input signal and said clock signal, and
   the timing of the injection of said pulses is responsive to said second control signals generated by said phase detector.

14. The system of claim 13 wherein
   said loop subsystem comprises an oscillator (20) for generating said clock signal, a loop filter (18) for providing a filtered third control signal for altering the frequency of said oscillator, and said source supplies said current pulses to said filter so as to generate said third control signal.

FIG. 1

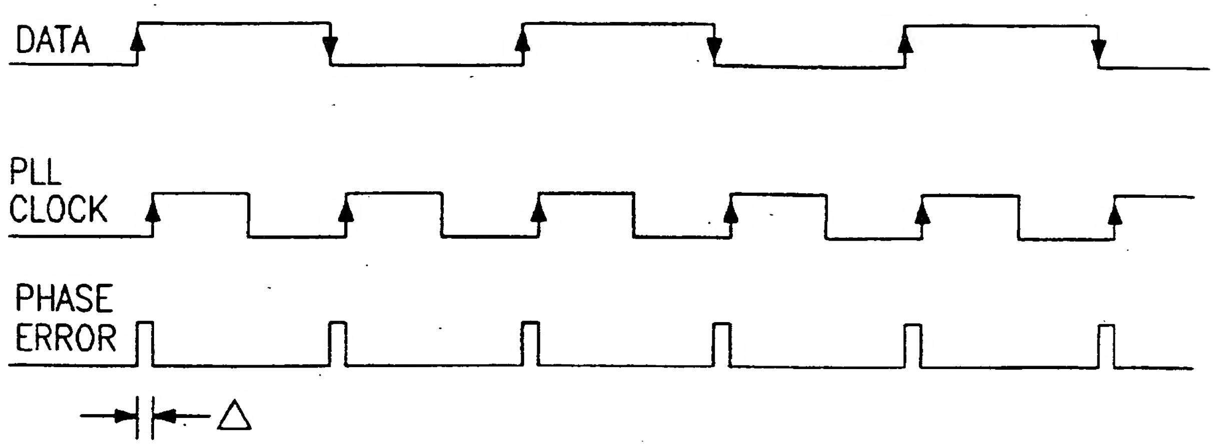
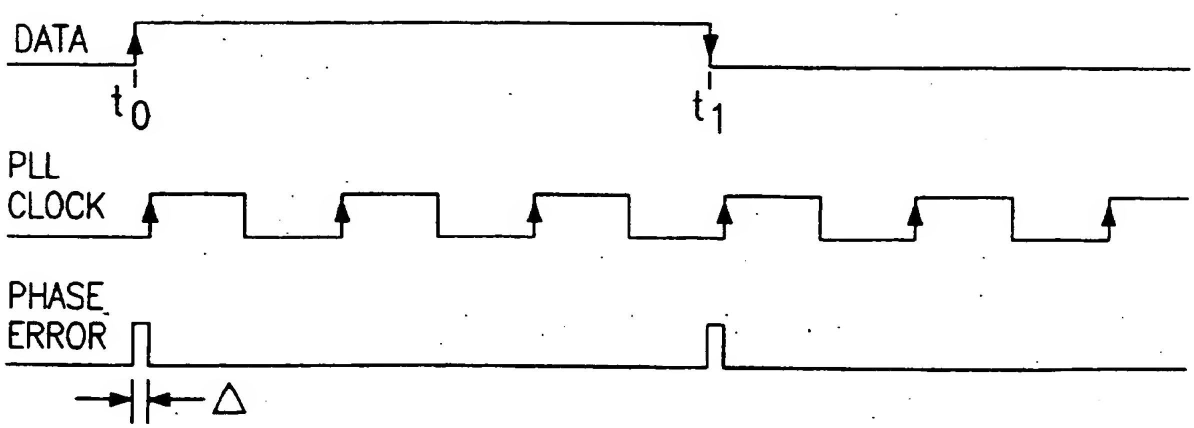

DATA
PLL
CLOCK
PHASE
ERROR
Δ

FIG. 2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t1
PLL
CLOCK
PHASE
ERROR
Δ

FIG. 3

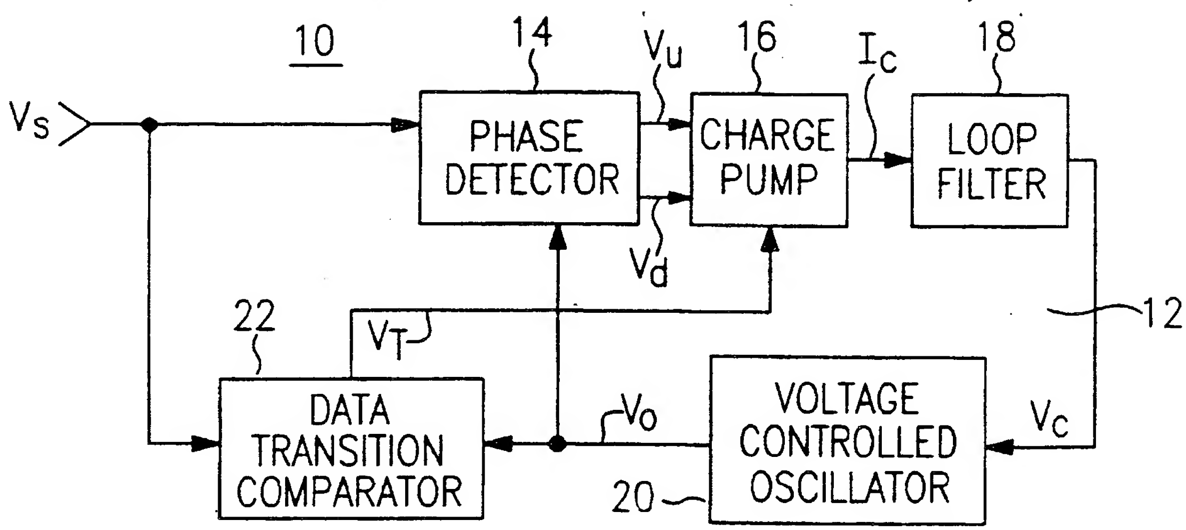
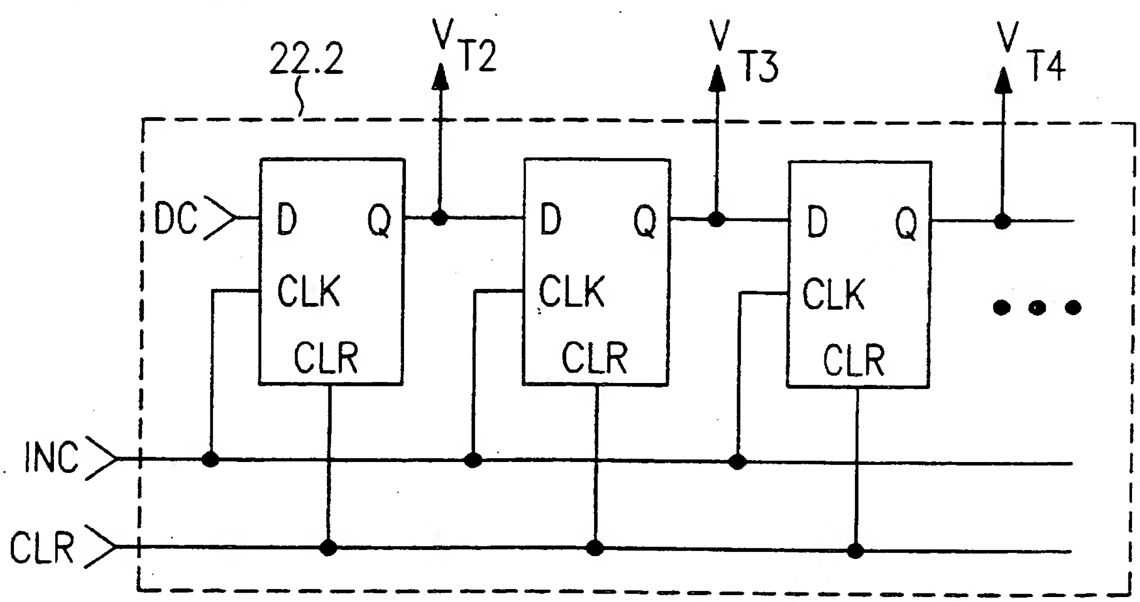
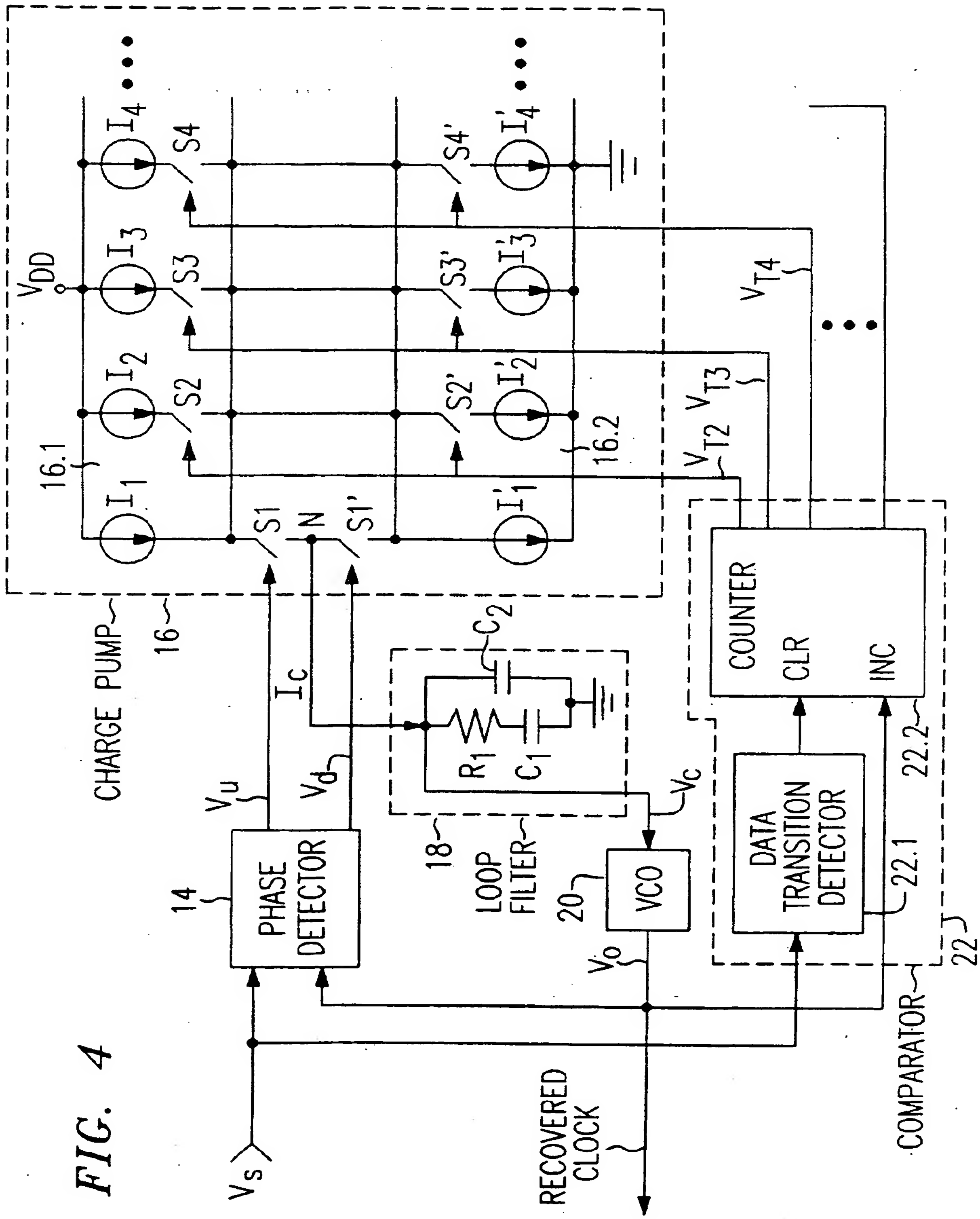

10
14
16
18
Vs
PHASE DETECTOR
CHARGE PUMP
LOOP FILTER
Vu
Vd
Ic
12
22
VT
DATA TRANSITION COMPARATOR
Vo
VOLTAGE CONTROLLED OSCILLATOR
Vc
20

FIG. 6


22.2
VT2
VT3
VT4
DC
D
Q
CLK
CLR
INC
CLR


CHARGE PUMP
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16.1
16.2
I_1
I_2
I_3
I_4
I'_1
I'_2
I'_3
I'_4
S1
S2
S3
S4
S1'
S2'
S3'
S4'
N
V_{T2}
V_{T3}
V_{T4}
I_c
C_2
R_1
C_1
V_u
V_d
V_c
14
PHASE DETECTOR
18
LOOP FILTER
20
VCO
V_o
V_s
RECOVERED CLOCK
COUNTER
CLR
INC
DATA TRANSITION DETECTOR
22.1
22.2
22
COMPARATOR

FIG. 4

FIG. 5

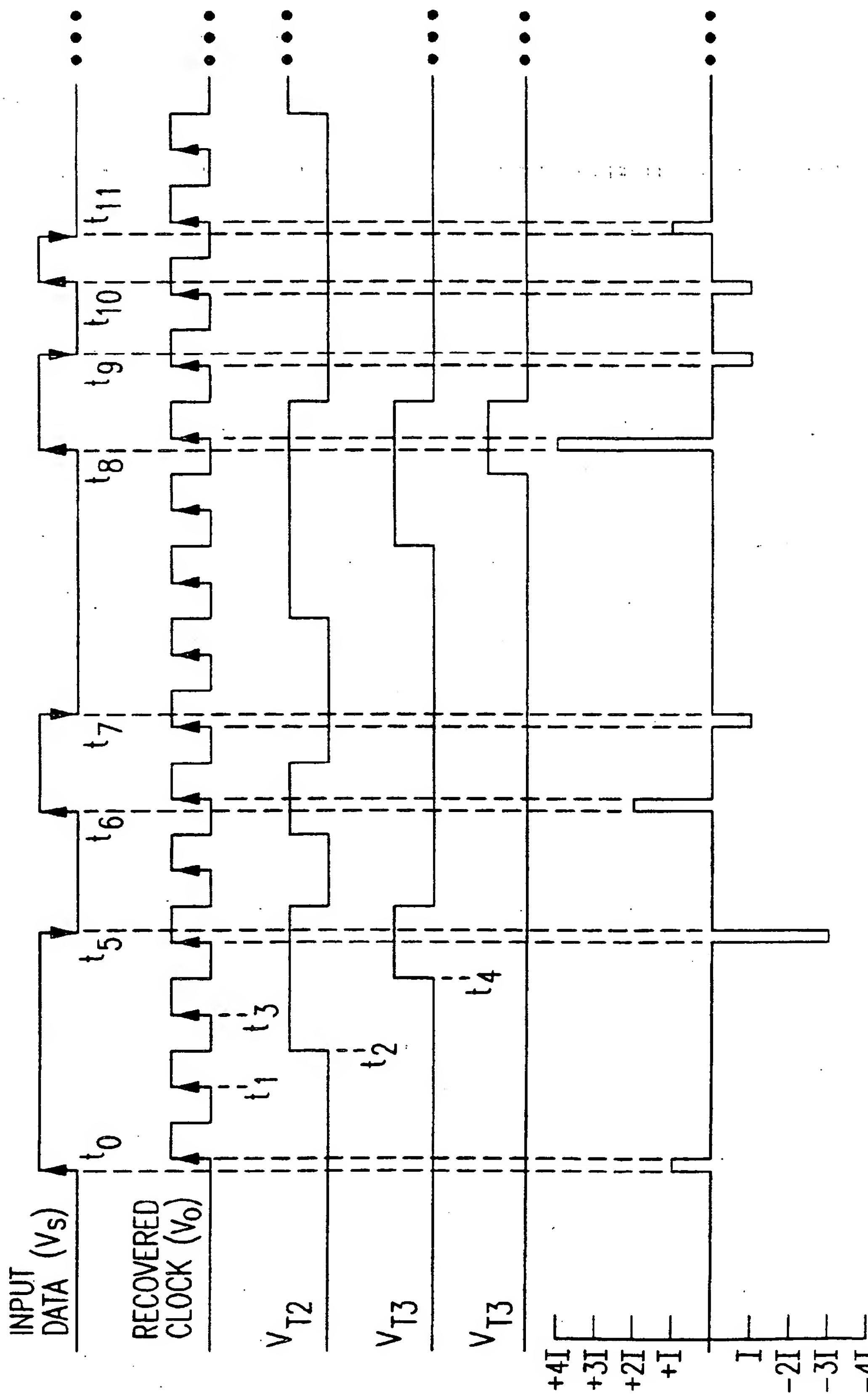

INPUT DATA (Vs)
RECOVERED CLOCK (Vo)
VT2
VT3
VT3
+4I
+3I
+2I
+I
I
-2I
-3I
-4I
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11

FIG. 3

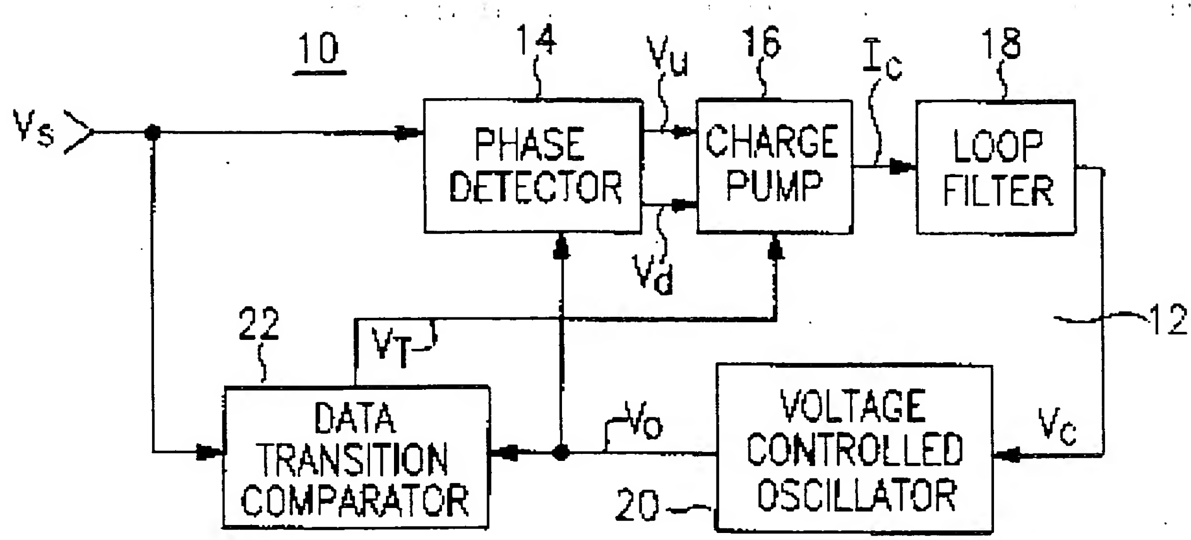

10
14
16
18
Vs
PHASE DETECTOR
Vu
Vd
CHARGE PUMP
Ic
LOOP FILTER
12
22
VT
DATA TRANSITION COMPARATOR
Vo
VOLTAGE CONTROLLED OSCILLATOR
Vc
20

FIG. 6

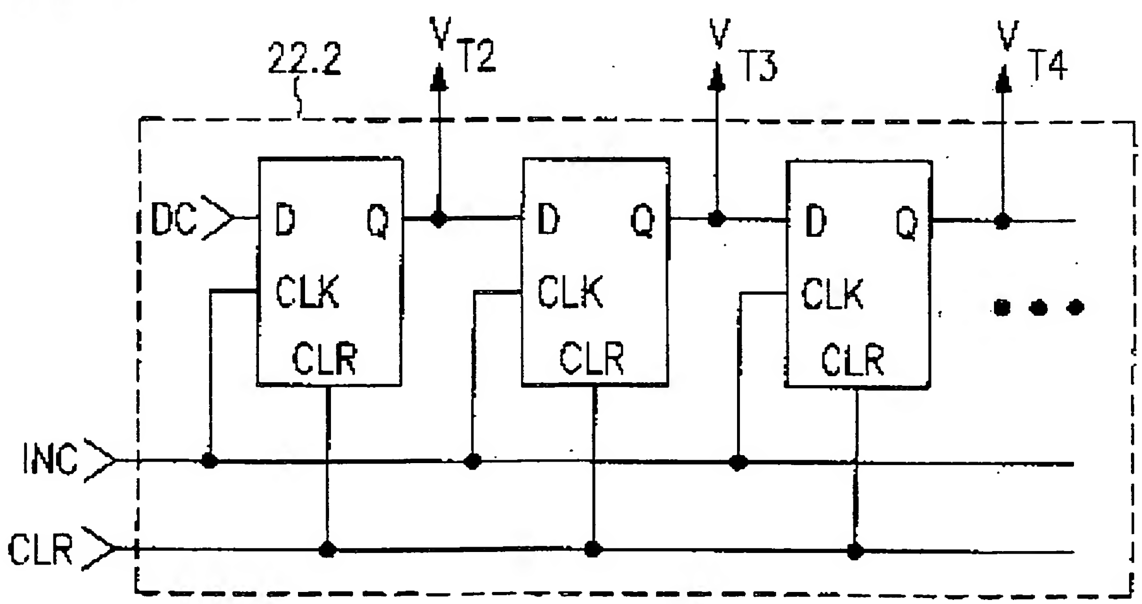

22.2
VT2
VT3
VT4
DC
D
Q
CLK
CLR
INC
CLR

FIG. 1

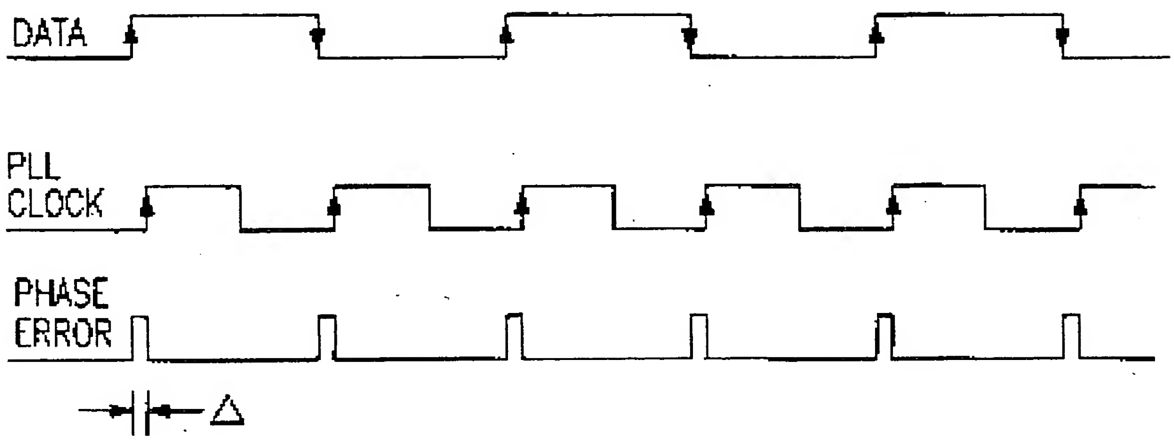

DATA
PLL
CLOCK
PHASE
ERROR
Δ

FIG. 2

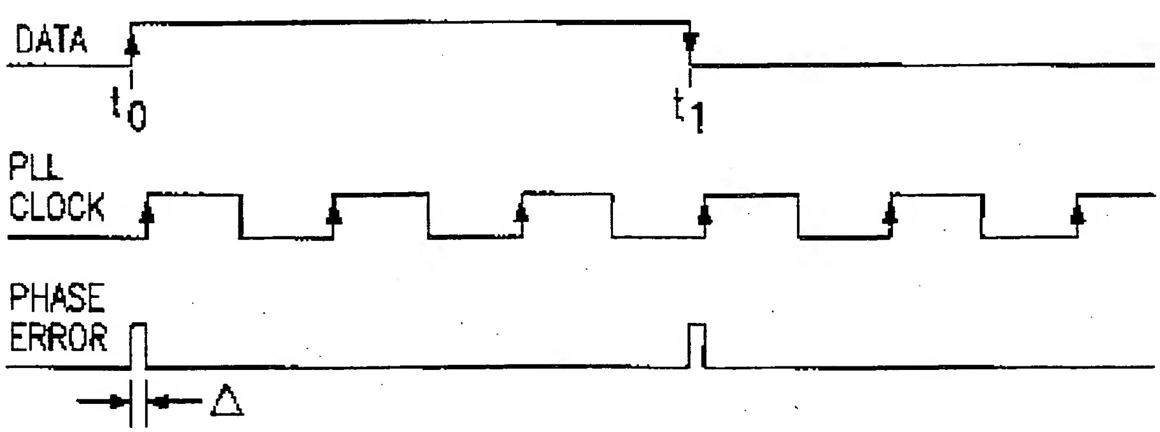
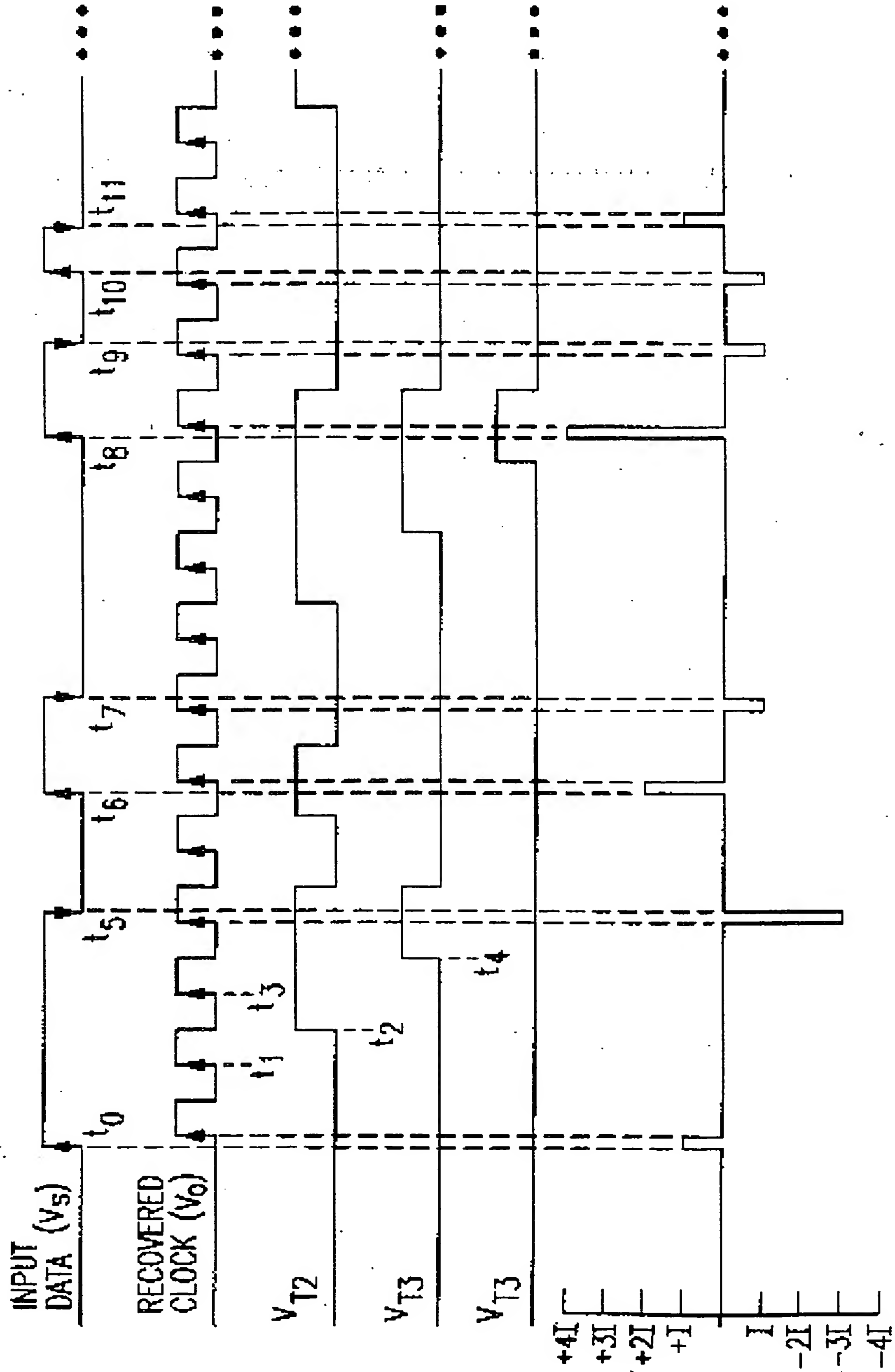

DATA
t_0
t_1
PLL
CLOCK
PHASE
ERROR
Δ

FIG. 5



INPUT DATA (Vs)
RECOVERED CLOCK (Vo)
VT2
VT3
VT3
+4I
+3I
+2I
+1I
I
-2I
-3I
-4I
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11

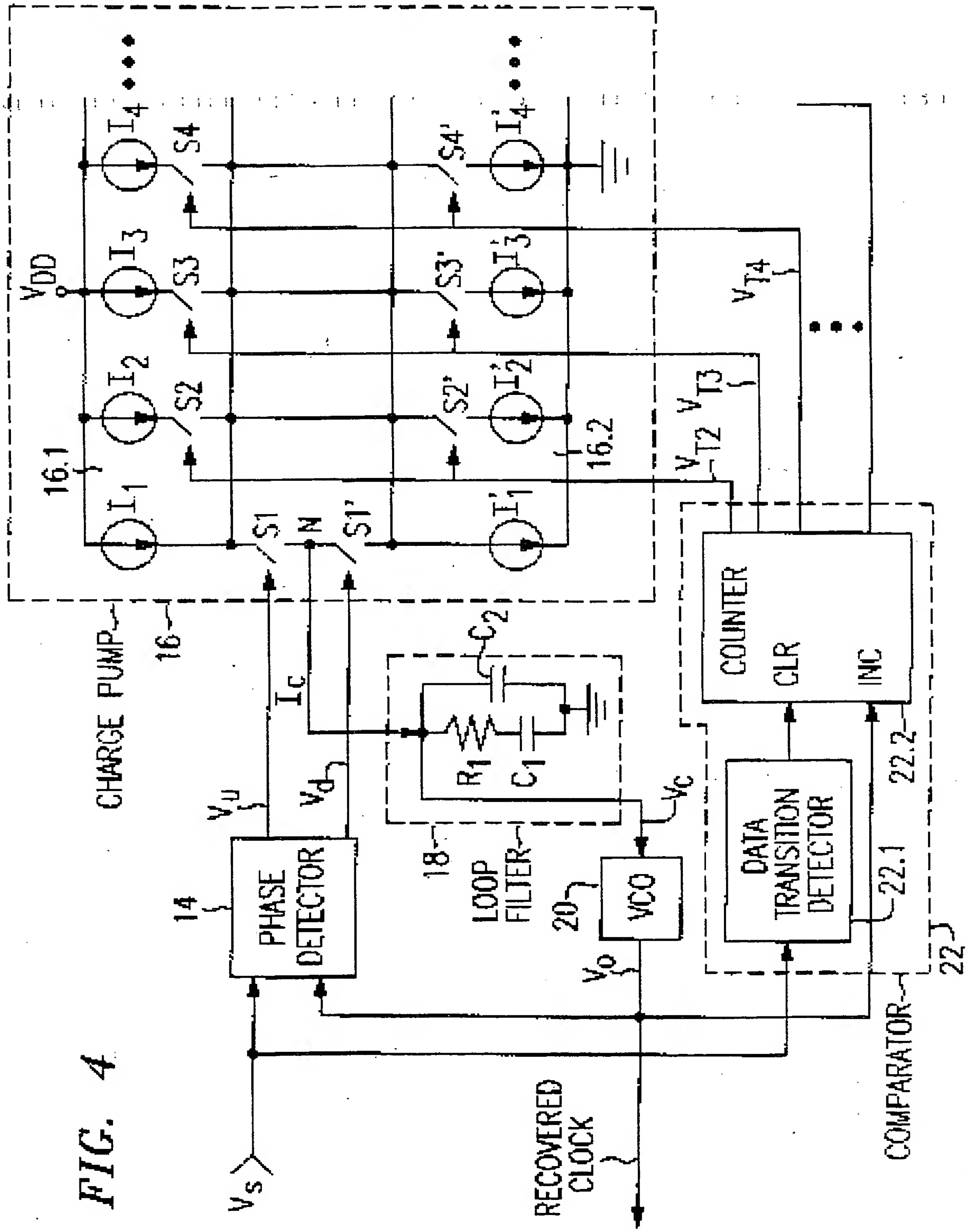

CHARGE PUMP
16
16.1
16.2
V_{DD}
I_1
I_2
I_3
I_4
I'_1
I'_2
I'_3
I'_4
S1
S2
S3
S4
S1'
S2'
S3'
S4'
N
V_{T2}
V_{T3}
V_{T4}
COUNTER
CLR
INC
DATA TRANSITION DETECTOR
22.1
22.2
22
COMPARATOR
PHASE DETECTOR
14
V_u
V_d
I_c
C_2
R_1
C_1
V_c
18
LOOP FILTER
VCO
20
V_o
V_s
RECOVERED CLOCK

FIG. 4

(19) Europäisches Patentamt
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(54) **Phase-locked loop system with compensation for data-transition-dependent variations in loop gain.**

(57) The loop gain of a phase locked loop (10) is made to be controllably responsive to the transition density of an input data signal. In one embodiment a charge pump (16), positioned between the phase detector (14) and the loop filter (18), supplies pulse-amplitude-modulated current pulses to the loop filter, the amplitude of pulses being related to the data transition density.

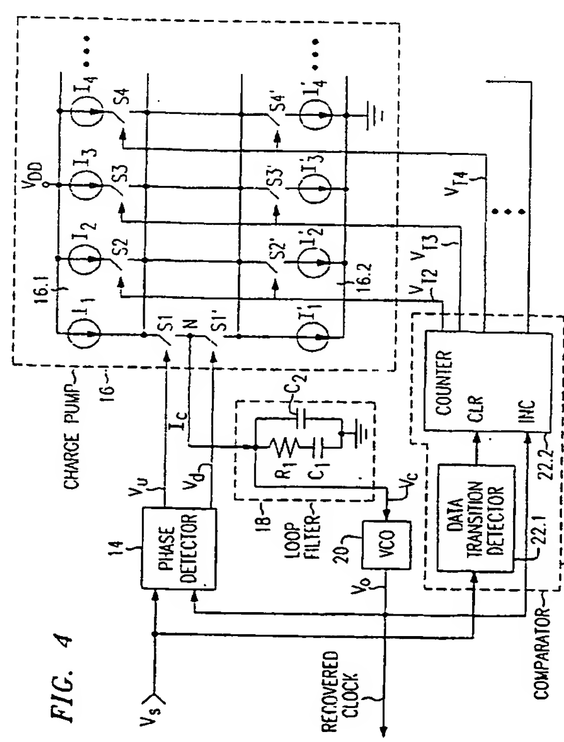

FIG. 4

EP 0 585 090 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 93 30 6642

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	FR-A-2 662 875 (R. BOSCH GMBH) * page 2, line 27 - line 32 * * page 6, line 9 - line 27 * * page 9, line 5 - line 16; figure 1 * * page 10, line 19 - page 11, line 22; figures 2,3 * * page 16, line 3 - page 18, line 12; figure 7 * ---	1-15	H03L7/089 H03L7/107
P,X	US-A-5 173 664 (C. PETERSON ET. AL.) * column 2, line 62 - column 3, line 35; figure 2 * ---	1	
A	US-A-4 926 141 (B. HEROLD ET. AL.) * column 2, line 9 - line 21 * * column 3, line 46 - column 4, line 34 * * column 7, line 59 - column 8, line 55; figures 2,4 * ---	1	
A	WO-A-91 07823 (TELEFONAKTIEBOLAGET LM ERICSSON) * page 7, line 30 - page 8, line 26; figure 4 * ---	1	TECHNICAL FIELDS SEARCHED (Int.Cl.5)
A	US-A-4 876 518 (G. PERKINS) * column 2, line 31 - column 3, line 63; figure 1 * -----	1	H03L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 November 1994	Butler, N

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